1   **Specification**

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3   **THERMAL GRADIENT ENHANCED CVD DEPOSITION AT LOW PRESSURE**

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5   **BACKGROUND OF THE INVENTION**

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7   This application is a continuation in part of U. S. Application Serial No. 09/396,588 filed

8 September 15, 1999 (which claims the benefit of U. S. Provisional Application Serial No.

9 60/100,594 filed September 16, 1998), which is a continuation in part of (a) U. S. Application

10 Serial No. 08/909,461 filed August 11, 1997, (b) U. S. Application Serial No. 09/228,835 filed

11 January 12, 1999 (which claims the benefit of U. S. Application Serial No. 60/071,572 filed

12 January 15, 1998), and (c) U. S. Application Serial No. 228,840 filed January 12, 1999 (which

13 claims the benefit of U. S. Provisional Application Serial No. 60/071,571 filed January 15,

14 1998). The disclosures of the foregoing applications are hereby incorporated by reference.

15

16 **Field of the Invention**

17   The present invention relates to methods and apparatus for chemical vapor deposition

18 onto a substrate, and more particularly to a method that deposits silicon at a high rate due to

19 enhanced mass transport by thermal diffusion, i.e., the "Soret effect", by using a temperature

20 gradient above the substrate surface.

21

22 **Description of the Prior Art**

23   The semiconductor industry has been depositing poly crystalline silicon for a number of

24 years. The method of choice for most applications is a Low Pressure Chemical Vapor

25 Deposition (LPCVD) process. The LPCVD process is a well studied art wherein poly crystalline

26 silicon deposition is accomplished by placing a substrate in a vacuum chamber, heating the

27 substrate and introducing silane or any similar precursor such as disilane, dichlorosilane, silicon

28 tetrachloride and the like, with or without other gases. The reactant gases are usually pre-heated

29 prior to passing over a wafer when a rapid deposition is required. The pre-heating pre-activates

30 the reactants and increases the rate of subsequent deposition. A disadvantage of this process is

1   that it causes gas reactions that deplete the supply of available reactants which partially defeats

2   the effect of pre-activation in increasing the deposition rate. Deposition rates of approximately

3   10 to 100 angstroms per minute are typical for low-pressure processes (less than 1 Torr) in a hot

4   wall low pressure reactor. Deposition rates of 20 to 300 angstroms per minute are achieved in a

5   vertical flow reactor with deposition rates as high as 500 angstroms per minute. Silicon

6   deposition rates over 10,000 angstroms per minute have been reported, however these high

7   deposition rates do not produce poly crystalline silicon films that are useful in manufacturing

8   semiconductor devices because the resulting poly crystalline silicon has undesirable features

9   such as large grain size, non uniform thickness, etc. Deposition rates of approximately 3000

10   angstroms per minute of useful semiconductor quality poly crystalline silicon are achieved with a

11   higher pressure process (25 to 350 Torr) as described in detail in United States Patent No.

12   5,607,724.

13   A typical prior art CVD system is illustrated in Fig. 1, and includes a reaction chamber 12

14   having a quartz tube 14. The chamber is enclosed on a first end by a seal plate 16 that can be

15   removed for installation and removal of a boat 18 carrying substrates 20. A reactant gas 22 such

16   as silane or similar precursor and hydrogen and a dopant gas such as phosphine are supplied to

17   the chamber 12 through ports 24 and 25 to tubing 27 and flow through the chamber 12 and exit

18   the exhaust port 26. A plurality of heater elements 28 are separately controlled and adjustable to

19   compensate for the well known depletion of feed gas concentration as the gas 22 flows from the

20   gas injection tube 27 to the exhaust port 26. The system of Fig. 1 typically operates at a gas

21   chamber pressure in the range from 100 to 200 mTorr, and at a gas flow rate from 100-200 sccm.

22   The reactant gas is usually silane diluted with hydrogen. Operating in the low pressure range of

23   100-200 mTorr with silane, or other similar precursor, results in a low deposition rate, typically

24   in the range of 10 to 100 angstroms per minute, and 5 to 30 angstroms per minute if a dopant gas

25   is introduced. The resulting surface roughness is typically 10 - 15 nm. Operation at higher

26   concentrations of the reactant gases results in non-uniform deposition across the substrates, as

27   well as large differences in the deposition rate from substrate to substrate. Increasing the gas

28   flow rate in the chamber of Fig. 1 can improve deposition uniformity at higher pressures, but has

29   the disadvantage of increasing the gas pressure resulting in gas phase nucleation causing

30   particles to be deposited on the substrate.

1   There are other problems associated with the reactor of Fig. 1, such as film deposition on

2   the interior surfaces of the quartz tube 14 causing a decrease in the partial pressure of the

3   reactive feed gas concentration near the substrate surface. This results in a reduced deposition

4   rate and potential contamination due to film deposited on the wall of tube 14 flaking off and

5   falling on the substrate 20 surfaces. Another problem occurs due to the introduction of a

6   temperature gradient applied between the injector end and exhaust end of the tube to compensate

7   for the depletion of reactive chemical species from the entrance to the exit. As a result of this

8   temperature gradient, the deposited poly crystalline silicon grain size varies from substrate to

9   substrate, i.e. across the load zone, because the grain size is temperature dependent. This

10   variation in grain size from substrate to substrate can result in variations of poly crystalline

11   silicon resistivity and difficulties with the subsequent patterning of the poly crystalline silicon

12   resulting in variations in the electrical performance of the integrated circuits produced.

13   A prior art vertical flow reactor 30 is illustrated in Fig. 2. This reactor is capable of

14   deposition rates as high as 500 angstroms per minute. The substrates 32 are placed in a substrate

15   carrier 34 in the reactor 30. The reactor chamber 36 is confined by a quartz bell jar 38 and a

16   seal plate 40. The bell jar 38 is surrounded by a heater 42 for heating the substrates 32 to the

17   required temperature. The reactant gases such as silane and hydrogen are introduced through

18   ports 44 and 46, and flow through the gas injection tube 48 to the injector 50, across the substrate

19   32 and out the exhaust port 52. The arrangement of Fig. 2 greatly reduces the gas depletion

20   effect experienced with the device of Fig. 1, and thereby allows an increased gas flow which

21   results in an increased deposition rate of up to 500 angstroms per minute. Two major problems

22   are associated with the apparatus of Fig. 2. In operation, the injection tube 48 and injector 50 are

23   at the same temperature as the substrates 32, a condition that results in silicon deposition in and

24   on the injection tube 48 and injector 50, which then flakes off and is deposited as particles on the

25   substrate 32. The other major problem is that the substrates 32 are not at the same temperature

26   due to the method of heating the substrates from heater 42 with no heater below the substrates.

27   The non-uniform heating causes a non-uniform silicon deposition over the substrates 32 as poly

28   crystalline silicon deposition is a surface reaction rate limited process, which is very temperature

29   dependent.

30   Fig. 3 shows a prior art single substrate reactor 54 that overcomes some of the problems

31   associated with the reactors of Figs. 1 and 2. This is described in detail in U.S. Pat. No.

1   5,607,724. A substrate 56 is placed on a rotating pedestal 58 in chamber 54. Upper lamps 62

2   and lower lamps 63 radiate energy through transparent chamber walls 64 and 66 to uniformly

3   heat the substrate 56. The pedestal 58 is turned to rotate the substrate 56, which is heated on

4   both sides by the lamps. The substrate temperature is therefore uniform over its surface, which

5   results in a uniform poly crystalline silicon deposition on the substrate 56. The reactor 54 does

6   not have an injector in the chamber, which eliminates the problem of deposition on the injector

7   50 shown in Fig. 2. The reactant gas 67 is supplied through an inlet port 68 and exits exhaust

8   port 70. The major problem associated with the reactor of Fig. 3 is the limited throughput, i.e.

9   the number of substrates processed per hour. This problem can be addressed by increasing the

10   operating pressure to 10 Torr or greater resulting in high deposition rates exceeding 1000

11   angstroms per minute, however operating the reactor at such high pressures can result in a gas

12   phase reaction where silicon particles are formed in the gas and deposited on the substrate.

13   Another problem associated with the reactor is the tendency for silicon deposition on the quartz

14   walls 64, 66 resulting in loss of radiant energy transmission from the lamps 62, 63. This causes

15   non-uniform heating of the substrate resulting in non-uniform film deposition on the substrate

16   56. Additionally, the silicon deposited on quartz wall 64 can flake off and fall onto the substrate

17   surface 56.

18   Current demands of semiconductor processing require rapid film deposition with uniform

19   and repeatable film thickness, and the smoothest film surface possible with controlled grain size.

20   In addition, the time the substrate is above 600° C must be held to a minimum, as heating the

21   substrate to elevated temperatures, i.e. greater than 600° C results in unwanted diffusion of

22   dopants. Because of this, a high deposition rate is important to reduce the time that the substrate

23   is above 600° C. Good film uniformity and repeatability is necessary to ensure consistent

24   electrical performance, and smooth films are required for sub-micron lithography processes.

25

26   **SUMMARY**

27   It is therefore an object of the present invention to provide a method and apparatus for the

28   Chemical Vapor Deposition (CVD) of various materials at a high rate.

29   It is a further object of the present invention to provide a method and apparatus for the

30   CVD of various materials at a high deposition rate with improved uniformity.

1   It is another object of the present invention to provide a method and apparatus for the

2   CVD of various materials at a high rate, with improved uniformity and reduced surface

3   roughness.

4   Briefly, a preferred embodiment of the present invention includes a method wherein a

5   substrate is placed in a reaction chamber and rotated to ensure uniform heating and a uniform

6   flow of reactant gases over the substrate surface. Upper lamps positioned above the substrate

7   and lower lamps below the substrate are activated to apply heat to an upper thermal plate and a

8   lower thermal plate which in turn heat the wafer upper and lower surfaces. The upper and lower

9   lamps are operated to raise the substrate temperature to 500-700° C for silicon deposition, or any

10   other temperature required for the deposition of other materials, and to provide a heat gradient

11   between the upper and lower thermal plates and thus cause a thermal gradient between the upper

12   substrate deposition surface and the upper thermal plate. This heat gradient causes a large

13   increase in the deposition rate for a given reactant gas flow rate and chamber pressure. The

14   preferred parameters for implementation of the present invention include the temperature of the

15   upper thermal plate adjusted to be 100-200° C above the temperature of the lower thermal plate,

16   the substrate temperature in the range of 400-700° C, the reactant gas pressure between 250 and

17   1000 mTorr, and the gas flow rate in the range of 200-800 sccm. The substrate rotation is

18   approximately 5 RPM, however the speed of rotation is not critical. For example, a deposition

19   rate of about 2000 angstroms per minute is achieved with a 100-200° C temperature differential

20   between the thermal plates, substrate temperature about 650° C, pressure of 250 mTorr and

21   silane flow of 500 sccm.

22   An advantage of the present invention is that it provides a higher deposition rate CVD

23   method with good film quality.

24   A further advantage of the present invention is that it provides a CVD deposition method

25   with a deposition rate five times more rapid than prior art methods providing comparable film

26   quality.

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28   **IN THE DRAWING**

29   Fig. 1 illustrates a prior art multi-substrate horizontal tube reactor;

30   Fig. 2 illustrates a prior art multi-substrate vertical flow reactor;

31   Fig. 3 shows an improved single substrate reactor with a rotatable pedestal;

1   Fig. 4 is a flow chart of the method of the present invention;

2   Fig. 5 is a cross-sectional view of a single substrate reactor for use in illustrating the

3   method of the present invention;

4   Fig. 6 is a graph of silicon deposition as a function of substrate temperature with and

5   without application of a temperature gradient;

6   Fig. 7 is a graph of silicon deposition as a function of silane flow;

7   Fig. 8 is a graph of silicon nitride deposition as a function of silane flow; and

8   Fig. 9 is a graph of silicon nitride deposition as a function of pressure.

9

10   **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

11   Referring now to Fig. 4 of the drawing, a preferred embodiment of the method of the

12   present invention is displayed in a flow chart. A substrate is placed 72 on a carrier in a reactor

13   chamber, and the carrier and therefore substrate are rotated 74. The substrate is heated 76 to a.

14   temperature to cause CVD, preferably between 500°C and 700°C, the heat being supplied by an

15   upper heater, heating an upper thermal plate positioned above the substrate top surface and a

16   lower heater, heating a lower thermal plate below the substrate bottom surface. The

17   temperatures of the upper and lower heaters are displaced to provide a thermal gradient between

18   the thermal plates, with the upper thermal plate preferably set approximately 100-200°C above

19   the temperature of the lower thermal plate. The thermal gradient is not critical, but preferably in

20   the range of 50-100°C per inch. An apparatus for achieving this will be described in reference to

21   Fig. 5, and includes thermal plates spaced above and below the substrate, with the plates each

22   spaced about one inch from the substrate. According to the method, the plates are heated

23   unequally so as to cause the temperature of the upper thermal plate to be 100-200°C above the

24   temperature of the lower thermal plate. Other methods for creating the thermal gradient will be

25   apparent to those skilled in the art, and these are also included in the spirit of the present

26   invention.

27   The process gas is then injected 78, preferably achieving a chamber pressure in the range

28   of 250 to 1000 mTorr. The gas is preferably injected at a rate of 200-800 sccm and at a velocity

29   greater than 100 cm/sec across the substrate surface, with the gas stream restricted to a narrow

30   region (0.5-1.5 inches) above the substrate. The process gas injection and temperature

31   conditions are then maintained for the length of time required to deposit the desired film

1 thickness, at which point a shutdown procedure 80 is implemented wherein the process gas is

2 turned off and evacuated from the chamber, and the rotation is stopped and the substrate

3 removed from the chamber.

4 The sequence of operations shown in Fig. 4 has some flexibility which will be apparent to

5 those skilled in the art. For example, the substrate can be heated to operating temperature prior

6 to beginning rotation, although this is not preferred. Similar variations are apparent in the

7 shutdown procedure. These and other variations that will be apparent to those skilled in the art

8 are included in the spirit of the present invention. The key element of novelty is the inclusion of

9 the thermal gradient above the substrate, preferably implemented with heated thermal plates

10 including one above and one below the substrate. The thermal plates can be heated directly with

11 embedded resistance heaters, or heated from lamps as will be described in reference to Fig. 5.

12 The addition of a high velocity gas stream passing across the substrate provides a source of gas

13 with a high concentration of the desired reactant species in contact with the surface of the

14 substrate, resulting in the deposition rate being surface reaction rate limited. The high velocity

15 gas injection is discussed in U.S. Patent Application Serial No. 09/396,588 filed September 15,

16 1999, the content of which is incorporated herein by reference.

17 The very high rate of deposition enabled by the present invention at relatively low overall

18 chamber pressures can move the reaction into the regime where the deposition rate approaches or

19 exceeds the crystallization rate, resulting in the growth of very small crystals and therefore very

20 smooth poly crystalline silicon films with a minimum surface roughness. The method can also

21 be used to accelerate the deposition of intrinsically slow processes such as α - Si.

22 The other advantage over conventional batch CVD systems is the reduced thermal

23 budget. As semiconductor device geometries are reduced to submicron sizes, the thermal budget

24 must be reduced accordingly. A hot wall CVD system requires the substrates to be at elevated

25 temperatures typically for two or more hours, while the present invention requires the substrate

26 to be at elevated temperatures typically for two to three minutes depending on the required film

27 thickness.

28 Referring now to Fig. 5, a reactor 82 is shown that can be adjusted to perform deposition

29 according to the present invention. A detailed description of this reactor is given in U.S. Patent

30 5,551,985. In reference to the reactor 82 of Fig. 5, the method of the present invention begins by

31 placing a substrate 84 on a carrier ring 86 that is supported by a rotatable heat plate 88. The

1   vacuum chamber 90 includes an outer wall 92 with an upper quartz window 94 attached, through

2   which heat is radiated from upper lamps 98 to heat the upper thermal plate 102 which radiates

3   heat to the top surface of the substrate 84. Lower lamps 100 radiate heat through a lower quartz

4   window 96 to the lower thermal plate 88 which radiates heat to the lower surface of the substrate

5   84. The upper lamps 98 control the temperature of the upper heat plate 102, and the lower lamps

6   100 control the temperature of the rotatable heat plate 88. In operation, the upper heat plate 102

7   is heated to a temperature approximately 100°C above the temperature of the lower heat plate 88.

8   Other temperature differences than 100-200°C are included in the spirit of the present invention,

9   as well as operational and construction alternatives such as having an upper heater and no lower

10 heater depending on the required temperature of deposition. The purpose for the temperature

11 difference in the plates is to provide a temperature gradient above the substrate deposition

12 surface, with the temperature increasing with the distance above the substrate deposition surface.

13 A preferred temperature gradient is in the range of 50 to 100° C per inch, with the temperature

14 increasing with distance from the deposition surface, which is the upper surface in the apparatus

15 as described in reference to Fig. 5. As mentioned above, a gradient could be achieved with only

16 an upper heater. The actual heater temperatures or thermal plate temperatures to achieve the

17 required gradient will vary depending on the particular chamber dimensions (such as thermal

18 plate position, etc.) used to implement the present invention.

19   In the reactor of Fig. 5, the substrate 84 reaches an equilibrium temperature

20 approximately half way between the temperature of the upper heat plate 102 and the lower heat

21 plate 88. The exact temperature of the substrate is very difficult to measure and is not relevant to

22 the practice of the present invention. The reactant gases are introduced to the chamber interior

23 by way of gas injector 104 and flow across the top surface of the substrate 84. The injector 104

24 may have a plurality of injector ports (not shown). The gases are preferably confined to a narrow

25 space 107 between the substrate 84 and upper heat plate 102. The injector is also preferably

26 oriented to direct the reactant gas 108 to impact on the deposition surface 109 of substrate 84,

27 which maximizes the gas concentration at the substrate surface 109 and contributes to a rapid

28 silicon deposition. In order to reduce unwanted deposition on the injector 104, the injector is

29 typically cooled. The details of the above apparatus, including a plurality of injector ports that

30 can be directed, as well as details for a water cooled injector are described in U.S. Patent

31 5,551,985, the contents of which is incorporated herein by reference. The reactant gases are

1 evacuated from the vacuum chamber through an exhaust port 106 by way of a vacuum pump (not

2 shown). An inert gas such as argon is injected between the upper quartz window 94 and the

3 upper heat plate 102 to prevent the reactant gases 108 from entering the space between the upper

4 quartz window 94 and the heat plate 102. An inert gas is also injected in the space between the

5 lower quartz window 96 and the bottom of the substrate 84 to prevent the entry of reactant gases

6 into that space.

7 The deposition time for a 3000 Angstrom layer of poly crystalline silicon is typically one

8 to two minutes, with operational conditions generally as indicated in Fig. 4. In comparison, if

9 the substrate is heated equally from top to bottom with all other process conditions held constant,

10 the deposition rate is reduced by a factor of 3 to 10 times or more.

11 Performance characteristics of the method of the present invention using the reactor of

12 Fig. 5 are illustrated in graphical form in Figs. 6 and 7. Fig. 6 has two curves for comparing the

13 deposition rate using the thermal gradient according to the present invention with the deposition

14 rate achieved using prior art uniform heating. Curve 112 shows, for example, that at 650°C the

15 use of gradient heating results in a deposition rate of approximately 2000 angstroms per minute

16 at 250 mTorr as compared with 400 angstroms per minute at 700 mTorr with uniform heating

17 according to curve 114. The deposition rate enhancement observed due to gradient heating is in

18 part due to the wafer temperature being higher compared to the case when it is heated equally

19 from top and bottom, but the majority of the deposition rate enhancement is due to the thermal

20 gradient established above the wafer. The difference between gradient heating and uniform

21 heating shown in Fig. 6 would even be greater if the deposition shown in curve 114 had been

22 done 250 mTorr instead of 700 mTorr. Fig. 7 shows the deposition rate as a function of silane

23 flow, demonstrating the importance of a high flow rate for rapid deposition.

24 Fig. 8 shows the deposition of silicon nitride obtained with thermal gradient heating in

25 the apparatus depicted in Fig. 5. Curve 116 is the deposition rate at 2000 mTorr versus curve

26 118 at 1000 mTorr. Fig. 9 shows the deposition rate for silicon nitride verses pressure with the

27 method of the present invention.

28 Although the present invention has been described above in terms of a specific

29 embodiment, it is anticipated that alterations and modifications thereof will no doubt become

1 apparent to those skilled in the art. It is therefore intended that the following claims be

2 interpreted as covering all such alterations and modifications as fall within the true spirit and

3 scope of the invention.

4   What is claimed is: